Translation

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference FPEL04150011	FOR FURTHER ACTION	See Form PCT/IPEA/416
International application No. PCT/CN2004/000375	International filing date *(day/month/year)* 19.Apr.2004(19.04.2004)	Priority date *(day/month/year)* 17.Apr.2003 （17.04.2003）
International Patent Classification (IPC) or national classification and IPC IPC7 G06F7/00		
Applicant Li,Zhizhong; Xu, juyuan		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of   3   sheets, including this cover sheet.

3. This report is also accompanied by ANNEXES, comprising:

   a. ☐ *(sent to the applicant and to the International Bureau)* a total of _____ sheets, as follows:
      ☐ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).

      ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.

   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic _____, containing a sequence listing and/or tables related thereto, in electronic form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:
   ☒ Box No. I   Basis of the report
   ☐ Box No. II   Priority
   ☐ Box No. III   Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   ☐ Box No. IV   Lack of unity of invention
   ☒ Box No. V   Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   ☐ Box No. VI   Certain documents cited
   ☐ Box No. VII   Certain defects in the international application
   ☐ Box No. VIII   Certain observations on the international application

Date of submission of the demand 01.Sept. 2004 （01.09.2004）	Date of completion of this report 04.Jul 2005 （04.07.2005）
Name and mailing address of the IPEA/CN The State Intellectual Property Office, the P.R.China, 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer A413 Telephone No. (86-10)62084990

Form PCT/IPEA/409 (cover sheet) (April 2005)

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/CN2004/000375

Box No. I	Basis of the report

1. With regard to the **language**, this report is based on:

    ☒ the international application in the language in which it was filed

    ☐ a translation of the international application into _____ , which is the language of a translation furnished for the purposes of:

    ☐ international search (Rules 12.3(a) and 23.1(b))

    ☐ publication of the international application (Rule 12.4(a))

    ☐ international preliminary examination (Rules 55.2(a) and/or 55.3(a))

2. With regard to the **elements** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

    ☐ the international application as originally filed/furnished

    ☒ the description:

    pages _____

    pages * ___1-25_____ as originally filed/furnished

    pages * _____ received by this Authority on ___01.Sept. 2004___

    pages * _____ received by this Authority on _____

    ☒ the claims:

    pages _____

    pages * _____ as originally filed/furnished

    pages * _____ as amended (together with any statement)under Article 19

    pages * ___26-29_____ received by this Authority on ___01.Sept. 2004___

    pages * _____ received by this Authority on _____

    ☒ the drawings:

    pages ___1_____

    pages * ___2_____ as originally filed/furnished

    pages * _____ received by this Authority on ___01.Sept. 2004___

    pages * _____ received by this Authority on _____

    ☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing.

3. ☐ The amendments have resulted in the cancellation of:

    ☐ the description, pages _____

    ☐ the claims, Nos. _____

    ☐ the drawings, sheets/figs _____

    ☐ the sequence listing *(specify)*: _____

    ☐ any table(s) related to sequence listing *(specify)*: _____

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

    ☐ the description, pages _____

    ☐ the claims, Nos. _____

    ☐ the drawings, sheets/figs _____

    ☐ the sequence listing *(specify)*: _____

    ☐ any table(s) related to sequence listing *(specify)*: _____

    * *If item 4 applies, some or all of those sheets may be marked "superseded."*

Box No. V   Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1.   Statement:

Novelty (N)	Claims	1-13	YES
	Claims		NO
Inventive step (IS)	Claims	1-13	YES
	Claims		NO
Industrial applicability (IA)	Claims	1-13	YES
	Claims		NO

2.   Citations and explanations (Rule 70.7)

(1)Documents incorporated by reference are the following:

D1:US6073149A

D2:CN1136680A

(2)The present invention relates to the field of digital engineering method and processor , it provides a new digital engineering method , improves   operational speed . The mixed Q N-ary and carry line of digital engineering method according to the present invention includes:A digital sign is added to every bit of the common Q N-ary digitals participating in the operation , there are k mixed N-ary digitals to participate in the operation , Sums up k mixed Q N-ary   at the same time. Adding by bit beginning with the lowest bit,i.e., at a certain bit , two digitals of the above described k digitals are taken and added to generate "addition by bit", and the sum is taken into the next operation layer as "partial sum", meanwhile the acquired "mixed digital carry" is put into the high-order bit which is close to the bit that is   any carry line of the next operation layer. The operations don't stop until it generates "mixed Q N-ary carry" line. Then the sum obtained by the last "addition by bit" is the result if   addition operation . The present provides a processor with mixed Q N-ary and carry line operation.

(3)D1 discloses a computational circuit for a multi-value addition comprising a parallel adder, an output adder, a quantizing portion and a logic conversion portion. Each of said parallel adders calculating an intermediate sum of corresponding digit of said two multi-value numbers and a carry. Each of said output adders adding said intermadiate sum output from said corresponding parallel adder and said carry output from said parallel adder of neighboring lower digit.

D2 discloses a multiplier for selectively performing an unsigned magnitude multiplication with a modified Booth algorithm for a multiplication operation. It include a selection unit which provides an extension bit for performing an unsigned magnitude multiplication in a signed magnitude multiplication which is expressed by a two's complement format, and a partial product generateor for performing a sign digit operation increased by the extension bit.

(4)Claim 1-13 meet the criteria set out in PCT Article 33(2)-(4).Because the method and processor deals with the mixed Q N-ary. Before operation, A digital sign is added to every bit of the common Q N-ary digitals participating in the operation. The prior art could realize addition by bit ,but could not realize using the mixed Q number system and using   "returning to zero" mechanism.